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Performance Study of Strain Engineered CMOS Inverter Logic Using Silicon Nanowire and Carbon Nanotube Field Effect Transistors

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Abstract

Various non-ballistic effects have significant impacts on the characteristics of nanoscale devices whose performance can be boosted by strain engineering. The effects of uniaxial compressive and tensile strains on Complementary Metal-Oxide-Semiconductor (CMOS) inverter circuits consisting of Silicon Nanowire Field-Effect-Transistor (SiNW-FET) and Carbon Nanotube Field-Effect-Transistor (CNT-FET) have been investigated in this paper. At first, a CMOS inverter circuit has been developed using single-walled CNT-FET and SiNW-FET. A comparative analysis of the transconductances of both types of devices along with their dependence on applied strain has been presented. Afterwards, Simmons direct tunneling effect has been observed for both strained and unstrained CNT-FETs. Simulation result signifies that strained CNT-FET inverter has lower gate leakage current than its unstrained counterpart. Finally, a comparison between the effects of strains on the velocity vs electric field characteristics for both SiNW-FET and CNT-FET has been studied. As switching delay time for a CMOS inverter circuit is related to the velocity saturation effect, a conclusion can be drawn from these curves that for SiNW-FET CMOS inverter, tensile strain increases the switching delay time whereas compressive strain decreases it for high applied field. Accordingly, for CNT-FET CMOS inverter, strain increases the switching delay time for specific chirality.

Keywords: inverter; strain; transconductance; direct tunneling; velocity saturation.

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1. Introduction

To meet the emergence of developing devices with superior performance and downsizing of the device industry, nanoscale devices are a promising candidate for developing transistors as well as logic gates. Carbon Nanotube (CNT) and Silicon Nanowire (SiNW) both have the potential to improve the performance of these nanotransistors for which they are good choices for fabrication and optimization of such nanodevices. Nanowires are considered as building blocks for the ultimate scaling of Metal-Oxide-Silicon (MOS) transistors. Use of nanowires has the potential to push devices until the most extreme boundaries of down-scaling due to their physical and geometrical properties [1]. Charge trapping behavior and tunable surface governed transport properties enable SiNWs to be used as metal-insulator-semiconductors and in field-effect-transistors, with further applications as nanoelectronic storage devices [2], in flash memory and logic devices as well as chemical and biological sensors [3,4].

Compared to solid nanowires, nanotubes have a more complex structure, necessarily one-atom-thick sheets of pure carbon. They are also one-dimensional materials but nanotubes are hollow. The properties of carbon nanotubes can vary greatly depending on how they are rolled up, a property called chirality. At present, ballistic Carbon Nanotube Field-Effect-Transistor (CNT-FET) is treated as one of the nanoelectronic devices that have immense prospective to be treated as a switching device for future which utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) structure. The strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electro-migration. In principle, both active devices (transistors) and interconnects can be made out of semiconducting and metallic nanotubes, respectively [5]. Carbon nanotubes have the potential to achieve more ballistic transport, tunable optical properties, high dielectric constants and crystalline insulators.

A previously developed model [6] for the ballistic nanotransistor, mainly developed for MOSFET, is the main framework of our analysis. This model has been extended to observe the strain effects on CNT-FET and SiNW-FET in this work. Application of strain can improve the performance of SiNW-FET and CNT-FET significantly which has been shown in previous research works. Mechanical strain can be applied to the SiNWs to engineer the band structure and reduce the transport effective masses, thus boosting the transport properties of ultimate SiNWs [7]. From the experimental point of view, the enhancement of the mobility (or the transconductance) under applied strain has been reported in SiNWs [8–11]. As a matter of fact, SiNWs can withstand large non-intentional strains due to oxidation or other processing steps (e.g. thermal stress) and can be stretched on purpose in flexible electronics. Effect of uniaxial strain has been discussed for both <001> and <110> oriented gate-all-around SiNW-FET where it has been concluded that uniaxial strain can significantly improve the carrier mobility in the channel [12]. In our work, the effects of uniaxial strain on CMOS inverter circuits having SiNW and CNT separately as channel materials for the transistors have been investigated.

For CNT-FETs, it has been shown that even a small amount of uniaxial (< 2%) or torsional (> 5 Deg) strain can significantly affect the performance of the device due to the variation of the bandgap and band structure limited velocity [13]. Semiconducting CNT channels with different chiralities are influenced in different ways by a certain applied strain. In general, a type of strain which produces a larger bandgap results in increased Schottky barrier

height, decreased band structure limited velocity, smaller minimum leakage current, smaller ON current and larger achievable I_{ON}/I_{OFF} ratio. The other type of strain that reduces the bandgap results in the opposite effect. Strain thus plays an important role in the electrical properties of CNT and has been a subject of strong research interest. The technique of applying mechanical strain to tune the band structure and reduce the transport effective masses had been applied previously in advanced logic devices and also been used in CMOS technologies.

The theoretical discussion for our simulation work is presented in section 2 where the approach behind our work is explained in details. Transconductance relates the electrical characteristic of a device i.e. the current through the output to the voltage across the input of the device which is significantly influenced by the application of strain. In this work, the ratio of transconductance with and without strain (both tensile and compressive) has been observed for both SiNW-FET and CNT-FET CMOS inverters which is illustrated in section 3. The use of thin gate dielectric films followed by the rapid growing demand of downscale device size increases leakage current from these ultra-thin gate oxides, thereby limiting the FET scaling. This gate leakage current is a key issue in the design of nanodimensional devices which is investigated with strain effects for CNT-FET CMOS inverter from the simulation results. Furthermore, the performance of short-channel devices is affected significantly by velocity saturation which reduces the transconductance in the saturation mode. At low lateral electric field, the electron drift velocity in the channel varies linearly with the electric field intensity but at higher field, phonon scattering effect dominates and reduces the carrier mobility making velocity no longer proportional to the applied field. An important criterion in the design of semiconductor devices is velocity saturation which has been explored in section 3 with strain effects for SiNW-FET (both tensile and compressive strains) as well as CNT-FET with specific chiral indices. From that result, effects of strain on switching delay time have been concluded for both SiNW-FET CMOS inverter as well as CNT-FET CMOS inverter owing to the fact that switching delay time is related to the saturation velocity of the transistors used in the circuit.

2. Methods

In this work, a SiNW-FET inverter and a CNT-FET inverter with metal-semiconductor Schottky barrier at both the source-channel and drain-channel contacts have been used. Here, gate oxide thickness of 1.5 nm, temperature at 300 K and source Fermi level position at 0.5 eV are considered where SiO_2 has been used as insulator and Si as substrate. According to Niquet and his colleagues [7], transistors with diameters ~3-10 nm have been recently fabricated and characterized on the course of scaling down of nanodevices to ultimate dimensions. In this work, diameter of 3.1 nm has been chosen as nanowires with this diameter have been considered for calculation of effective density of states previously [14]. For CNT, diameter is kept same as SiNW to compare the characteristics of these two types of transistors. As short channel is a topic of interest, all of our works have been done for 10 nm channel length. For the simulation purpose, 78 points have been considered for both SiNW and CNT and the structure used is gate-all-around.

According to the theory of ballistic nanotransistors [6], a non-equilibrium mobile charge is induced between the source and the drain if electric field is applied. The positive charge densities in source, negative charge densities in drain and equilibrium charge densities are related to the density of states and Fermi-Dirac probability distribution. The induced drain current can be determined by [15]

$$I_{DS} = \frac{2qkT}{\pi\hbar}\left[F_0\left(\frac{U_{SF}}{kT}\right) - F_0\left(\frac{U_{DF}}{kT}\right)\right]. \quad (1)$$

Here, F_0 is the Fermi integral of order 0, k is the Boltzmann constant, ħ is the reduced Planck constant, T is the temperature, U_{SF} and U_{DF} are the potentials induced by terminal voltages at source and drain respectively as defined by

$$U_{SF} = E_F - qV_{SC}\,. \quad (2)$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS}\,. \quad (3)$$

where E_F is the Fermi level, V_{SC} is the self-consistent potential and V_{DS} is the induced voltage between drain and source. Although this model accounts for ballistic transport of the carriers, it has been upgraded to observe and analyze the effects of tensile and compressive strains on both SiNW-FET and CNT-FET CMOS inverters.

Effects of strain on the mobility of the carriers have been previously studied by Niquet and his colleagues [7]. The orientation of SiNW has significant impacts on its properties. Shiri and his colleagues [14] observed that bandgap change (60 meV to 100 meV) occurs for every 1% axial strain for <100> and <110> nanowires, respectively. This bandgap change is independent of nanowire size. It has also been studied that the nature of bandgap changes from indirect to direct due to the application of external strain. The change in effective density of states in the conduction band can be numerically simulated as [14],

$$N_c = \sqrt{\frac{2kT}{\pi\hbar^2}}\sum_{i=1}^{N} e^{E_c - \frac{E_i}{kT}}\sqrt{m_i^*}\ . \quad (4)$$

where m_i^* is the effective mass of sub-band *i*, E_i and E_c denote the bottom of sub-band *i* and the lowest conduction sub-band respectively, kT is the thermal energy (25.9 meV at T = 300 K) and N is the number of sub-bands within $Ec \pm 3kT$. The number of sub-bands in this $3kT$ window increases with nanowire diameter. As a result, effective density of states is higher for the nanowires with larger diameter.

Application of strain changes the bandgap in case of carbon nanotube. Extra bandgap caused by the shape distortion effect has a significant impact on the transport characteristics. The rate of change of bandgap can be expressed as [15]

$$\frac{dE_{g_{strain}}}{d\chi} = 3\sigma(1 + r_0)\, sign\,(2p + 1)\cos(3\varphi). \quad (5)$$

Here, $dE_{g_{strain}}$ is the gap shift due to the strain, χ is the distortion factor under strain, σ is the overlap integral of the tight-binding C–C model (~ 2.7 eV), $r_0 \approx 0.2$ is the Poisson's ratio and φ is the chiral angle of the nanotube. For a CNT with the chirality (n, m), $n - m = 3l + p$, where l and p are both integrals. The value of p is -1 if $mod(n - m, 3) = 2$ and $+1$ if $mod(n - m, 3) = 1$.

In this study, Simmons direct tunneling gate leakage current has been investigated in a thin gate oxide of CNT-FET structure. The increasing gate current (I_G) with ultrathin gate oxides at low voltages is a key issue limiting

the MOSFET scaling [16]. Direct Tunneling dominates for thinner gate oxides whereas Fowler-Nordheim tunneling becomes significant for thicker gate oxide. A crucial parameter affecting I_G is the effective barrier height (φ_{eff}) of the oxide embedded with nanotubes. According to the Simmons model, the tunneling current density through a thin barrier in the direct tunneling regime $\left(V < \frac{\emptyset_b - E_0}{q}\right)$ is given by [17]

$$J_D = \left(\frac{e}{4\pi^2 \hbar d^2}\right)\left\{\left(\emptyset_b - E_0 - \frac{eV}{2}\right) exp\left[-\frac{2(2m_{eff})^{\frac{1}{2}}}{\hbar} \times \alpha\left(\emptyset_b - E_0 - \frac{eV}{2}\right)^{\frac{1}{2}} d\right]\right\} - \left(\emptyset_b - E_0 + \frac{eV}{2}\right)$$

$$\times exp\left[-\frac{2(2m_{eff})^{\frac{1}{2}}}{\hbar} \times \alpha\left(\emptyset_b - E_0 + \frac{eV}{2}\right)^{\frac{1}{2}} d\right] \quad (6)$$

where m_{eff} is the electron effective mass, d is the barrier width, $\emptyset_b$ is the barrier height, V is the applied gate bias and α is a unit-less adjustable parameter that is called the actual polarizability which can be determined from the unscreened linear polarizability α_0 (α_0 is quadratically proportional to the tube radius R where the value of proportionality constant is 1.96 for metallic and 2.15 for semiconducting) and dielectric constant $\in_{CNT}$ as

$$\alpha = \frac{\alpha_0}{\in_{CNT}} \quad (7)$$

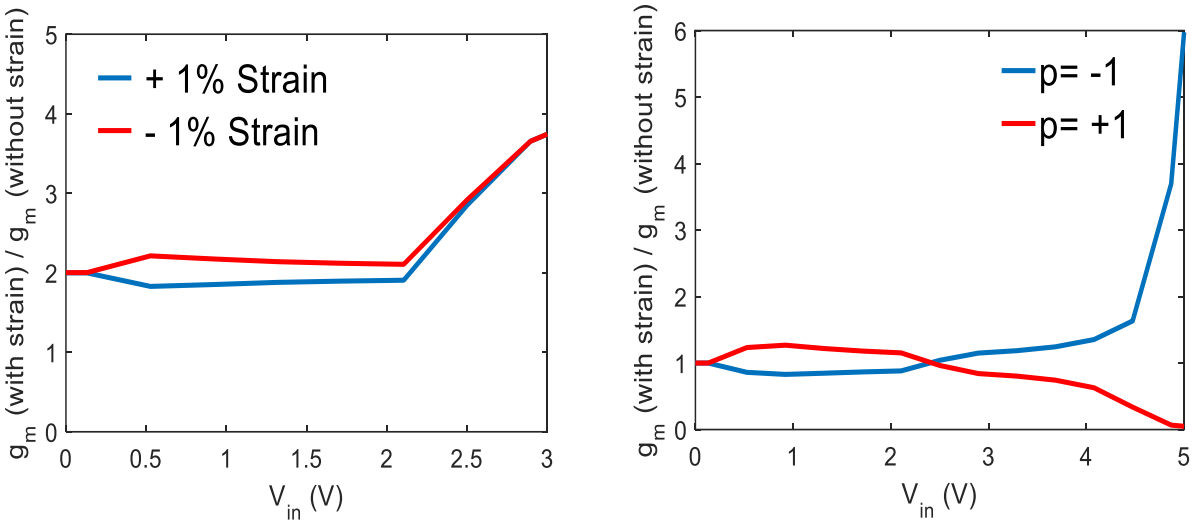
$$\alpha_0 = CR^2 \quad (8)$$

$$\in_{CNT} = 1 + 2\frac{\alpha_0}{R^2} \quad (9)$$

3. Simulation Results

In a CMOS inverter circuit consisting of a pull-up transistor (p-type) and pull-down (n-type) transistor, the input is applied at the gate terminals of both the complementary transistors which acts as a common node whereas the output is measured at the common drain terminal of both the transistors. In this work, as carbon nanotube and silicon nanowire have been used as channel regions replacing the conventional MOSFET inverters, the output current must be different for the same input voltage for both CNT-FET and SiNW-FET inverters.

While comparing Silicon Nanowires (SiNWs) with Carbon Nanotubes (CNTs), it has been noted previously that the slope of the bandgap vs strain changes rapidly with diameter in CNTs. But for SiNWs, it is independent of the orientation. Also, robust direct-indirect bandgap transition is absent in CNTs. For SiNWs, the abovementioned phenomena can be explained by the change in the effective density of states. Tensile strain decreases the density of states function N_{1D} and the decrease of N_{1D} will increase the output current. As a result, transconductance (g_m) is increased as shown in Figure 1(a). Compressive strain also increases g_m where the effect is slightly more than tensile strain. For carbon nanotube channel inverter, two types of chiralities have been considered. At first, the chirality (n, m) where $mod(n - m, 3) = 2$ is taken into account. In this case, the value of p from (5) is -1 and bandgap is decreased. From the simulation result as shown in Figure 1(b), the ratio of g_m for strained CNT to that



(a) SiNW-FET CMOS inverter

(b) CNT-FET CMOS inverter

Figure 1: Ratio of g_m for strained to g_m for unstrained SiNW-FET and CNT-FET CMOS inverters vs applied voltage. Here, +1% strain denotes tensile strain whereas −1% strain denotes compressive strain (Figure 1a) and the values of p signify two different types of chiralities as explained in section 2 (Figure 1b).

for unstrained one is < 1 for low input voltage whereas the ratio is > 1 for high input voltage. For CNT with $mod(n-m,3)=1$, the value of p becomes +1. This chirality increases the bandgap which in turn decreases transconductance for higher input voltage.

From the simulation results, it is obvious that for strained (both tensile and compressive strain) SiNW-FET based inverter, device transconductance is improved more significantly than that of strained CNT-FET based inverter. Both the inverters have almost similar physical size as the same parameter values have been considered. The gain (A_v) is directly related to the transconductance (g_m) which implies the fact that higher g_m means higher A_v. So, strained SiNW-FET can be a better choice than strained CNT-FET for the design of CMOS inverter to improve its overall gain.

In this work, Simmons direct tunneling has been studied for both strained and unstrained CNT-FETs. For unstrained CNT-FET, gate leakage current is seen to be higher than strained CNT-FET, more significantly for the input voltage greater than 1 V (Figure 2). The difference of gate leakage currents between the strained and unstrained condition depends on CNT chirality (n,m). For the case when the value of p from (5) is -1, that is $mod(n-m,3)=2$, the difference is significant. But for the case when $p=+1$, strained and unstrained CNT-FET has almost same gate leakage current with a slight deviation for high input. This comparison implies that strained CNT-FET inverter is a better choice than the unstrained one if the scaling down problem is required to be reduced as it results in decreased leakage current. Since devices with 10 nm channel length have been considered here in order to implement the short-channel devices, there is a trade-off between gate leakage current and overall device performance. This trade-off requires further investigation in future.

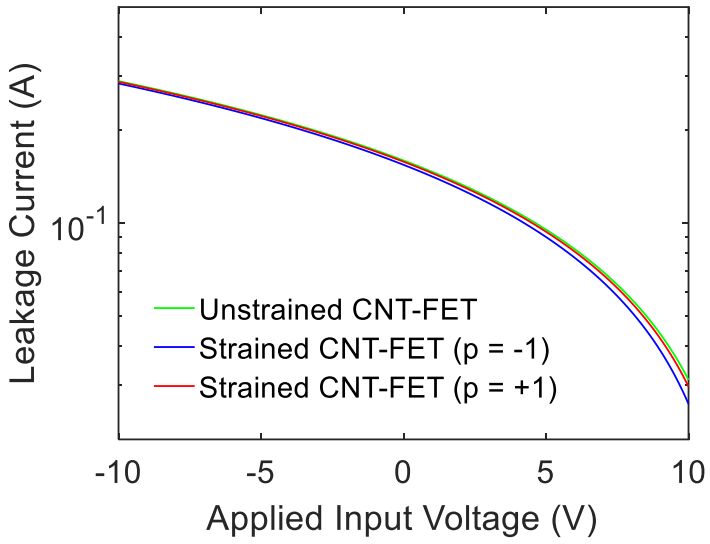
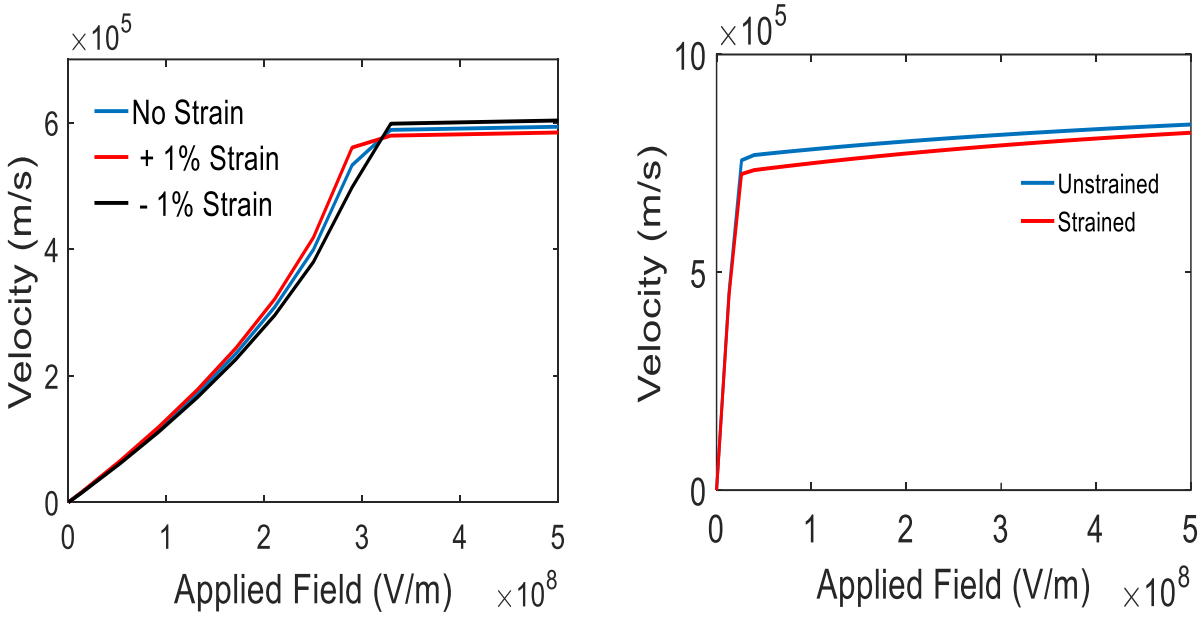


Figure 2: Direct tunneling gate leakage current for strained and unstrained CNT-FETs, here the value of p has been explained in (5) of section 2.

The present focus of discussion will be the effects of tensile and compressive strains on the velocity vs applied electric field characteristics of SiNW-FET. Here, simulation has been performed for a simple SiNW-FET from which the switching delay property for SiNW-FET CMOS inverter is concluded. Tensile strain tends to increase the mobility of the carriers and compressive strain tends to decrease it. Consequently, velocity is seen to be higher with tensile strain and lower with compressive strain for low applied electric field (Figure 3a). Although tensile



(a) SiNW-FET

(b) CNT-FET

Figure 3: Velocity vs applied electric field characteristics for SiNW-FET (Figure 3a) and CNT-FET (Figure 3b) under different strains.

strain increases the carrier velocity for low applied field, it causes the velocity to get saturated for high electric field at a relatively lower value. This can be explained by the fact that tensile strain increases the length of the nanowire and decreases its diameter. This type of change in the physical appearance results in scattering effect. Higher optical phonon scattering lowers the saturation velocity which is the underlying explanation behind the low saturation velocity for SiNW-FET with tensile strain. On the other hand, compressive strain causes lower phonon scattering as it not only increases the diameter but also decreases the channel length. As a result, better saturation velocity at higher electric field is possible for applied compressive strain although it causes lower carrier velocity at small applied field. Hence, compressive strain is preferable for higher applied fields whereas tensile strain improves the device performance for low fields for SiNW-FETs. In case of CNT-FETs, saturation velocity is reduced if strain is applied (Figure 3b). In this case, the chirality (n, m) is considered in such a way that $mod(n - m, 3) = 1$ i.e. the value of p is $+1$. This chirality increases the bandgap which in turn decreases the drain current for which velocity gets saturated at a lower electric field value. The insights from this discussion yield that the switching delay time can be reduced if compressive strain is applied on SiNW-FET CMOS inverters. On the

Table 1: Factors affected by strain for both SiNW-FET and CNT-FET

Affected Factors	SiNW-FET	CNT-FET
Transconductance of CMOS inverter, g_m	Improved for both tensile and compressive strain; improved by a factor which is higher than that for CNT-FET.	**At low voltage:** Improved for the chirality (n, m) such that $mod(n - m, 3) = 1$ and degraded for $mod(n - m, 3) = 2$. **At high voltage:** Degraded for the chirality (n, m) such that $mod(n - m, 3) = 1$, and improved for $mod(n - m, 3) = 2$.
Direct tunneling gate leakage current	Future research scope.	Reduced for both types of strain.
Saturation velocity	**At low applied field:** Tensile strain increases carrier velocity whereas compressive strain decreases it. **At high applied field:** Compressive strain increases saturation velocity whereas tensile strain decreases it.	Reduced for the chirality (n, m) such that $mod(n - m, 3) = 1$.
Switching delay for CMOS inverter	Reduced for compressive strain and increased for tensile strain.	Increased for the chirality (n, m) such that $mod(n - m, 3) = 1$.

contrary, the application of tensile strain on SiNW-FET CMOS inverters will result in the increase of this delay time which is less desirable. Similar increase in switching delay time occurs for CNT-FET CMOS inverters which is dependent on chiral vector. The effects of strain on different parameters for both SiNW-FET and CNT-FET are summarized in Table 1.

The major limitation of our work was the lack of experimental data. For bandgap of carbon nanotube, only data for certain chiral vectors from previous works have been used. Moreover, abrupt junction approximation was considered for the FET structures in this work for simplicity.

4. Conclusion

To sum up, the transconductances for both SiNW-FET and CNT-FET CMOS inverter logic gates are affected due to the applied tensile and compressive strains. For SiNW-FET inverter, both types of strains (tensile and compressive) increase the transconductance where the increase for compressive strain is slightly higher. On the other hand, for CNT-FET inverter, strain can both decrease and increase the transconductance for the same input voltage, depending on the nature of chiralities. The comparison yields that SiNW-FET inverter is more affected by strain than CNT-FET inverter, where the transconductance is comparatively higher for the former. So for the purpose of achieving higher gain, SiNW-FET CMOS inverter can be a better choice than CNT-FET CMOS inverter. From the next part of the simulation, it has been shown that for device scaling down of conventional FET structures, strained CNT-FET is the better choice than the unstrained one due to the reduction in direct tunneling gate leakage current for thin gate oxide. From the last part of the simulation, it can be concluded that although tensile strain improves the mobility of the carriers, it causes lower saturation velocity due to higher phonon scattering effect in SiNW-FET. On the contrary, compressive strain is preferable for higher saturation velocity at higher applied electric field. This implies that compressive strain has the potential to reduce switching delay time for SiNW-FET CMOS inverter. The application of strain results in the degradation of saturation velocity depending on the chirality for CNT-FET. As a result, switching delay is increased for CNT-FET CMOS inverter upon the application of strain depending on the chiral indices. According to these observations, a proper mechanical strain can be applied to achieve the best possible output from a CMOS inverter.

5. Recommendations

CMOS inverter modeling using SiNW-FET and CNT-FET has a wide number of areas which can be further explored. In future, CMOS inverter circuit using double-walled CNT-FET can be analyzed and compared with that of single-walled CNT-FET. Furthermore, Simmons direct tunneling effect can be observed for SiNW-FET and compared with that of CNT-FET. In addition, gate leakage current along with switching delay properties can be experimentally verified for both types of CMOS structures. The scope for future extension makes this work a promising one for the near future.

Acknowledgement

The basic FETToy 2.0 model has been used in this work which is available online [18].

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